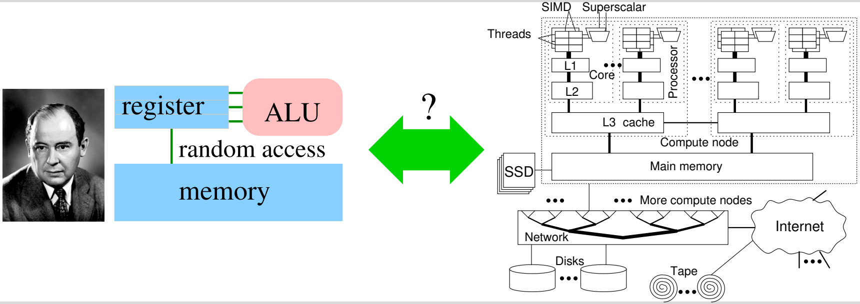
Karlsruhe Institute of Technology

Taming the Zoo of Parallel Machine Models

SPAA Tutorial

Peter Sanders | Jun 17, 2024



Overview

From von Neumann to modern machines

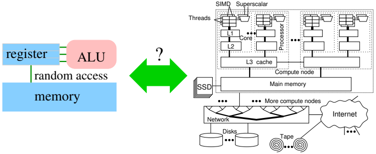
- RAM
- PRAM
- Memory hierarchies
- Distributed memory & communication
- Relations between models

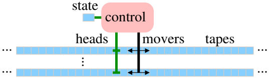
More abstract models

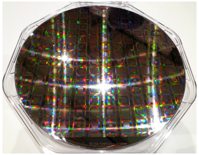
- MapReduce
- Distributed graph algorithms

Wrap Up

- GPU, Quantum, and more
- Open problems
- Future models

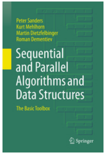






Sources

- Chapter Machine Models in 1st volume of my book Algorithm Engineering Draft:
  https://ae.iti.kit.edu/documents/people/sanders/aeModels.pdf
- My (parallel) algorithms textbook [SMDD19]
- My lecture on parallel algorithms



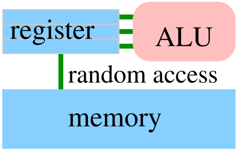
What is a (good) Machine Model

Abstraction of computations that allow (asymptotic) analysis of the resource consumption of algorithms

- Preferably simple
- Preferably close to reality

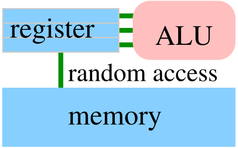
$\neq$ programming model
(which lacks performance aspect)

$\neq$ performance model
(which is much more detailed,
often more specific to a particular problem)



Random Access Machines (RAM)

(modern variant of the *von Neumann Model*) [SS63, SMDD19]



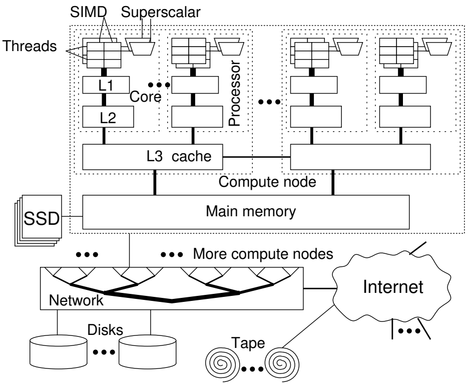
Sequential algorithms

- Count machine instructions
- on words of size $\mathrm{O}(\log n)$ for input size n, i.e. allow word/bit parallelism.

Still the basis for much of algorithmics.

The Problem

Modern machines are vastly different:



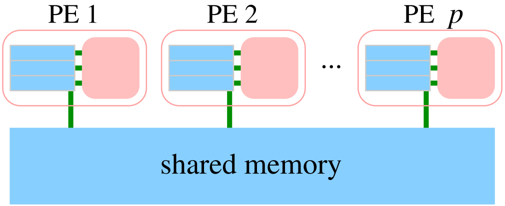
many forms of parallelism, complex memory hierarchies,...

Challenge: reconcile precision and simplicity

A Simple Parallel Model: PRAM
Parallel Random Access Machine

Idea: change RAM as little as possible.

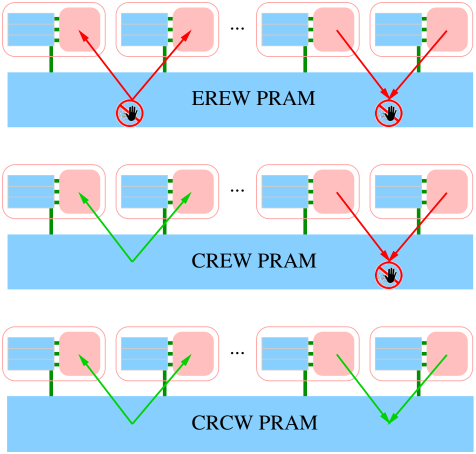
- p PEs (**P**rocessing **E**lements); numbered $1..p$.
  Every PE knows p and its own number.
- One machine instruction per clock cycle and PE – synchronous
- Shared global memory



Basic PRAM Variants

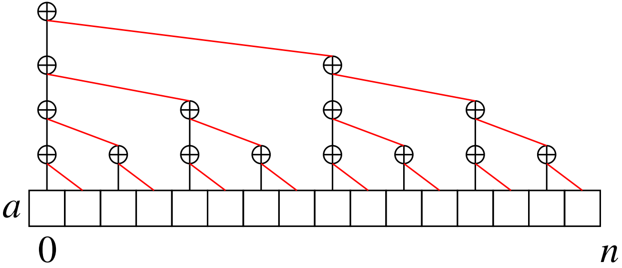
Concurrent access: Allow access by multiple PEs to the same memory cell in the same step?
Concurrent=yes, Exclusive=no.
Read or Write.

- EREW PRAM:
  Exclusive-Read, Exclusive-Write PRAM
  most restrictive
- CREW PRAM:
  Concurrent-Read, Exclusive-Write PRAM.
  Kind of default since
  caches approximate concurrent read well.
- CRCW PRAM:
  Concurrent-Read, Concurrent-Write PRAM.
  further variants regarding how conflicts are resolved (common, arbitrary, priority, combine)



Example: Reduction of Array $a[0..n)$

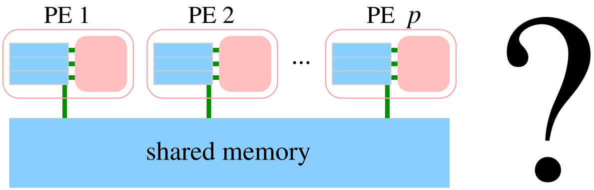
PE index $i \in \{0, \ldots, n-1\}$
active := 1
for $0 \leq k < \lceil \log n \rceil$ **do**
    if active **then**
        if bit k of i **then**
            active := 0
        else if $i + 2^k < n$ **then**
            $a[i] := a[i] + a[i + 2^k]$



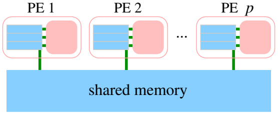
Criticism of PRAM

PRAMs were THE parallel model in the 1980s.
Parallel processing fell “out of favor” in the mid 1990s
(many bankruptcies of companies, era of “just wait for faster sequential processors”).
The PRAM model was seen as part of the problem.

- Unrealistic assumptions? Too fine-grained, hard to realize physically, lockstep execution is unrealistic,. . .
- Lack of transfer into applications
- Theoretical algorithms often look very different from what is done in applications
- Research ran out of interesting problems?



In Defence of PRAMs



!

In retrospect the criticism was largely unfair.

- PRAMs are very natural first step to express parallelism in computations.
- Many efficient PRAM algorithms can be further developed into efficient realistic algorithms.
- Todays many-core CPUs and GPUs are much closer to PRAMs than the first parallel computers (e.g., #cores, memory channels).
- Other now popular models such as MRC seem much farther removed from reality than PRAM.
- Surprisingly many open problems are left.

The actual problems were

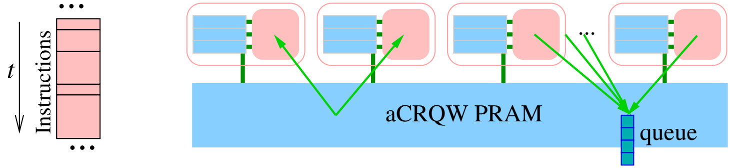
- Coarse complexity theoretic goal of polylogarithmic time and polynomial work ($\Rightarrow$algorithms can be highly inefficient)
- Lack of algorithm engineering

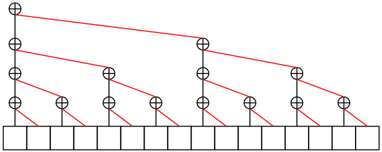
For example, my results on shortest paths [MS03b], matchings [BOS$^+$13], sampling [SLH$^+$18, HS22], or suffix arrays [KSB06], can be naturally explained using PRAM models.

Asynchronous PRAMs

aCRQW PRAM:

asynchronous Concurrent-Read, Queued-Write PRAM [GMR98, GMR99, SMDD19].
Programs must be correct regardless how long it takes to execute an instruction.
Write access takes time k when k PEs concurrently access a cell.
Uses atomic operations like fetch-and-add or compare-and-swap (CAS).
$\Rightarrow$ adequate modelling of contention.

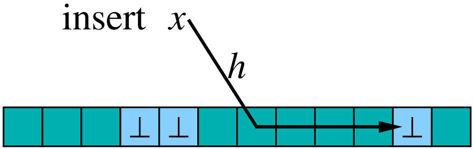




Exercise: What happens with our reduction example?

Example: Concurrent Hash Tables

Linear Probing [MSD19, SMDD19] largely does the job.



- Constant expected time for find – contention does not appear in practice as concurrent accesses are covered by cached copies.
- Constant expected time for insert – contention is unlikely.
- Update can suffer from contention.
- Maintaining a global variable for size kills performance of insert.

Open Problem:
Scalable Concurrent Algorithms and Data Structures

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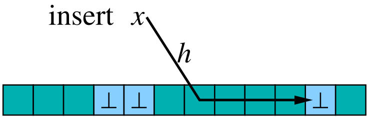
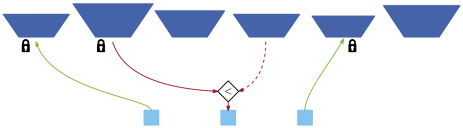
There is a large body of very important work on concurrent algorithms and data structures (in particular lock-free/wait-free) that is lacking a scalability analysis (or provably scalable variants).
I believe aCRQW-PRAM or related models can be a good basis here.



hash table



priority queue

The Work-Span Model

Abstract from the actual number of processors p [AB16, BFGS20] used for a computation.
Only look at the

work W performed and the

span (or depth) T_∞ i.e., the longest sequence of dependent operations.
$\approx$ time with unbounded # of PEs.

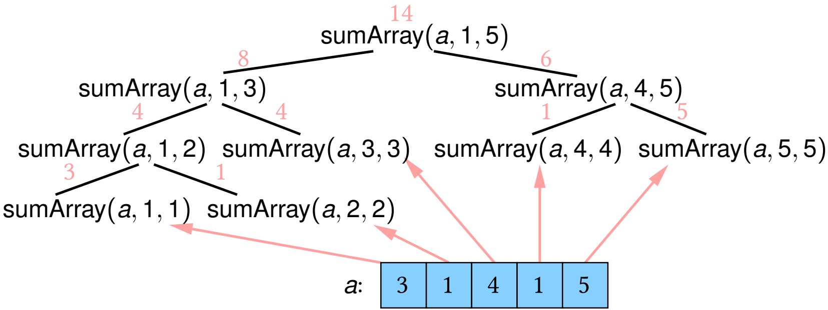
Computation $=$ graph of dependencies.
Unfolds at running time ($\neq$ circuit models)
Use fork operations to spawn tasks and atomic shared-memory operations
(e.g. CAS on aCRQW PRAM).

Example

Function sumArray$(a : \text{Array}, i, j)$ // compute $\sum_{k=i}^{j} a[k]$

  if $i = j$ **then return** $a[i]$

  else return sumArray$(a, i, \lfloor \frac{i+j}{2} \rfloor)$+ sumArray$(a, \lfloor \frac{i+j}{2} \rfloor + 1, j)$



Load Balancing for Forking Programs

Roughly: Using a work-stealing load balancer [BL99, SMDD19], the aCRQW PRAM can run programs in the work span model in expected time

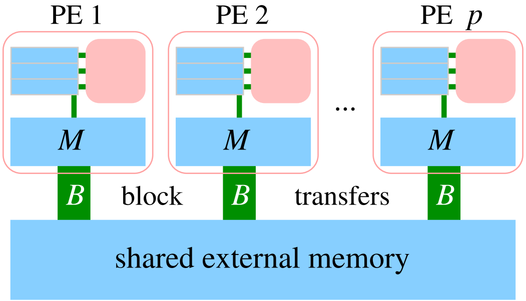
$$T(p) = \frac{\overbrace{W}^{\text{work}}}{p} + \overbrace{T_\infty}^{\text{span}}$$

(But check details of the model, e.g., what kind of forking)

Test-of-Time Award SPAA 2024

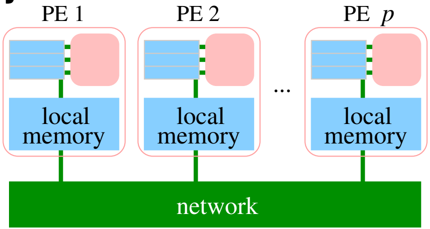
Parallel External Memory (PEM)

Any PRAM can be augmented to model a 2-level memory hierarchy [AGNS08].

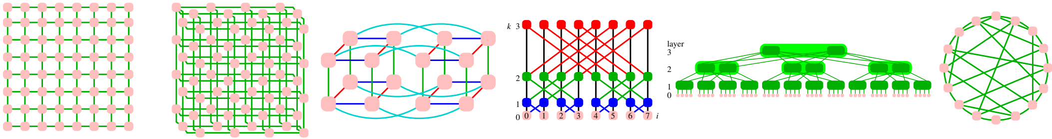


Count (parallel) I/O steps (in addition to internal work).
Example: cache-efficient parallel sorting [AFSW22].

Distributed-Memory Models



- Conceptually as simple and natural as PRAM
- We need a cost model for communication.
- Here: Abstract away the concrete network topology
  which was highly popular in the early days of parallel computing [Lei92].



Bulk Synchronous Parallel (BSP)

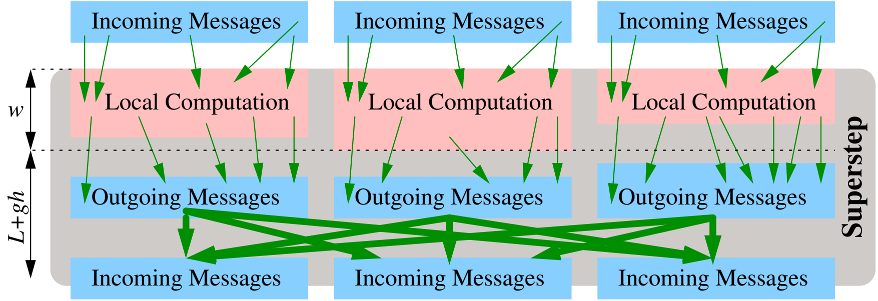
Decompose computation into synchronized supersteps [Val94]

L Latency (includes global synchronization)

g gap – measures network throughput

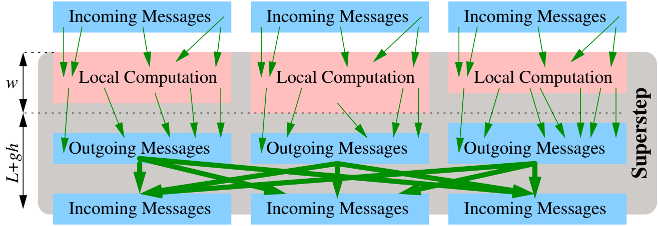
h bottleneck communication volume (*h*-relation)

w max. local work



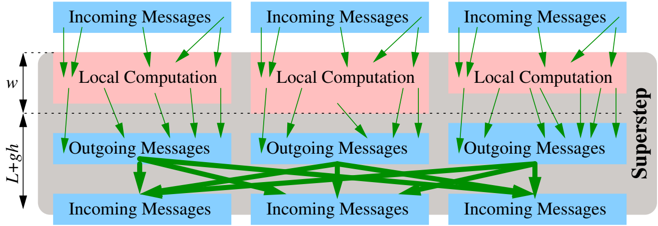
BSP: Strengths and Weaknesses

- + widely used
- + supported by some libraries
- – global synchronization is as expensive as other common primities such as broadcast, reduction, prefix sum which all take a logarithmic number of supersteps
- – too little differentiation of communication patterns, e.g., wrt average message size, locality
- – In practice, think of L as a huge value growing linearly with the number of PEs p!
- Special case CGM (Coarse Grained Multicomputer) – only count rounds



BSP$^+$: Fixing Some Weaknesses [SS24]

- Define h in terms of packets of size B rather than using machine words (BSP* [BDadH95]).
- Allow the collectives broadcast, reduce, prefix sum within a single superstep (anyway part of BSP libraries).



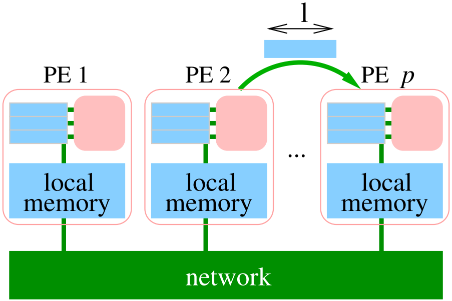
Asynchronous Distributed Memory: Point-to-Point Communication (P2P)

Time for sending a message of length ℓ [FL94, CHPvdG07, SMDD19]:

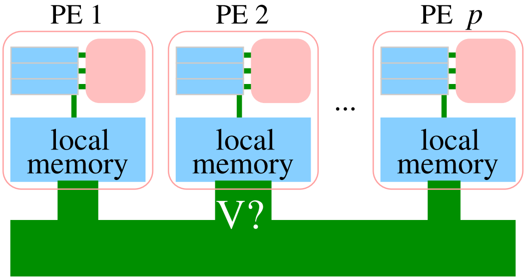
$$T_{\text{comm}} := \alpha + \beta\ell$$

Each PE can progress on one send and one receive at any point in time (full duplex).
(Several variants, e.g., either or = half duplex)

+ simple
+ asynchronous
+ defacto standard in practical distributed-memory computing
+ more useful parameters than the related LogP [CKP+93] model (see also LogGP model [AISS97])
− less known in theory community



Communication Efficient Algorithms

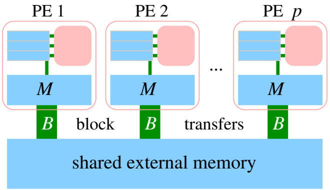


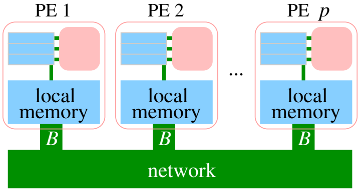
Owner computes paradigm:
Minimize bottleneck communication volume V.
Can we achieve volume sublinear in the local computation time?
Can we achieve polylogarithmic span?

Examples: duplicate detection [SSM13], linear programming [SSM13], top-k problems [HS16], graph generation [FLM$^+$19]

Relations Between Models

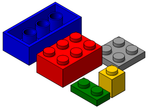
- All PRAM variants as well as BSP, P2P can emulate each other with at most logarithmic slow-down (assuming $L \subseteq \mathrm{O}(\log p)$, $\{g, \beta, \alpha\} \subseteq \mathrm{O}(1)$).
- BSP$^+$, P2P with $\ell = B = \alpha/\beta$ and PEM seem closely related.
  However, studying communication efficient algorithms with PEM would require you to assume that the input resides in the local memories.





Thus, decision for a particular model often is a matter of taste or you are interested in looking at parameters like α as variables rather than constants.

Model Lego



Use different models for different aspects of your algorithm.
Deal with hierarchical and heterogeneous architectures.
For example, parallel sorting [AFSW22]:

- BSP for a distributed memory sample sort
- PEM for a node-local shared memory sorter and partitioner
- specialized modelets to deal with branch mispredictions [KS06, SW04] or associative caches [MS03a]

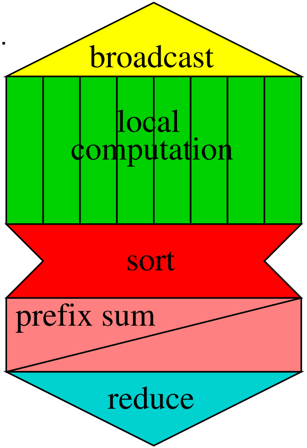
Much cleaner than one all-encompassing model.

Model-Agnostic Algorithm Design

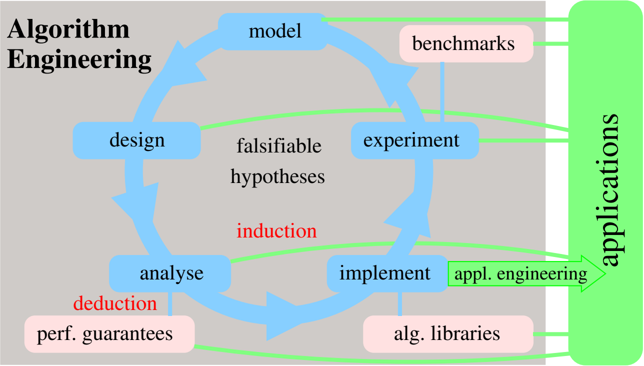
Construct your algorithm from building blocks like
broadcast, reduction, prefix sum, permutation, sorting, hash tables,. . .

Then plug in analysis for different models.

Model-Bingo in examples from my work:
random permutation [San98],
matching [BOS+13],
sampling [SLH+16]



Machine Models in Algorithm Engineering



pick initial model(s)
design
implementation takes care of unmodelled features
experiments may cause changing the model

Overview

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- Distributed memory
- Relations between models

More abstract models

- MapReduce
- Distributed graph algorithms

Wrap Up

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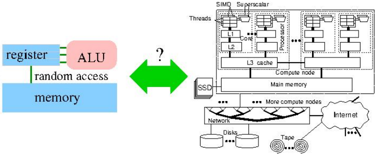
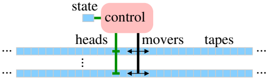
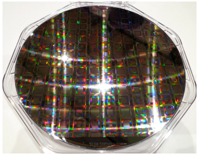
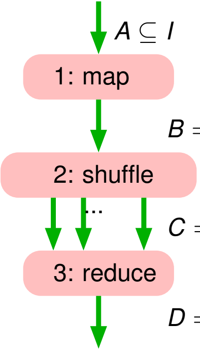
- Open problems
- Future models







MapReduce



$$A \subseteq I$$

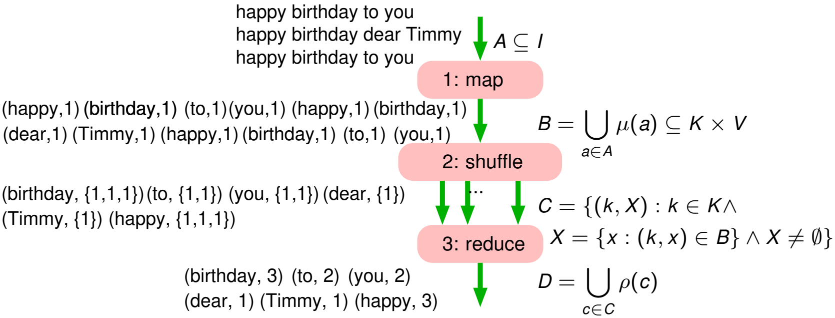
$$B = \bigcup_{a \in A} \mu(a) \subseteq K \times V$$

$$C = \{(k, X) : k \in K \wedge X = \{x : (k, x) \in B\} \wedge X \neq \emptyset\}$$

$$D = \bigcup_{c \in C} \rho(c)$$

[DG08]

MapReduce Example: Word Count



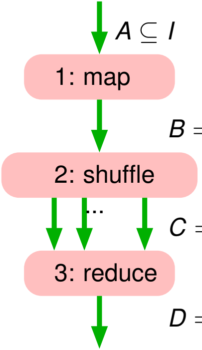
MapReduce Discussion

$+$ Abstracts away difficult issues

- parallelization
- load balancing
- fault tolerance
- memory hierarchies
- ...

$-$ Large overheads

$-$ Limited functionality



$A \subseteq I$

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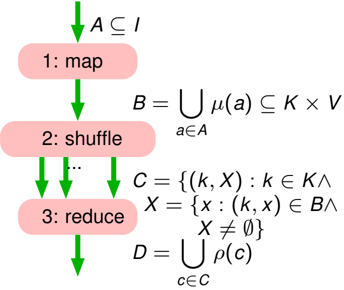
$$D = \bigcup_{c \in C} \rho(c)$$

MapReduce MRC Model

A problem is in MRC [KSV10] iff for input of size n:

- solvable in $\mathrm{O}(\mathrm{polylog}(n))$ MapReduce steps
- μ and ρ evaluate in time $\mathrm{O}(\mathrm{poly}(n))$
- μ and ρ use space $\mathrm{O}\left(n^{1-\epsilon}\right)$ ("substantially sublinear")
- overall space for B $\mathrm{O}\left(n^{2-\epsilon}\right)$ ("substantially subquadratic")



Roughly: count steps, (good for coarse grained complexity theory)
very loose constraints on everything else

MapReduce MRC Model **Criticism**

A problem is in MRC iff for input of size n:

- solvable in $\mathrm{O}(\mathrm{polylog}(n))$ MapReduce steps
- μ and ρ evaluate in time $\mathrm{O}(\mathrm{poly}(n))$ — n^2? n^{42}? “big” data?
- μ and ρ use space $\mathrm{O}\left(n^{1-\epsilon}\right)$ (“substantially sublinear”)
- overall space for B $\mathrm{O}\left(n^{2-\epsilon}\right)$ (“substantially subquadratic”) — “big” data?

Roughly: count steps,
very loose constraints on everything else — speedup? efficiency?

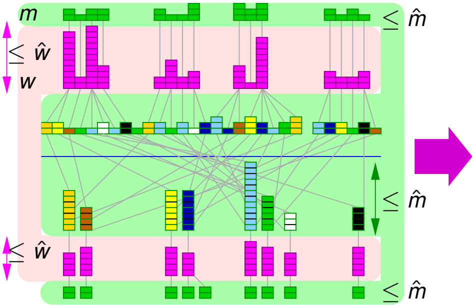
Sounds a bit like the problem that afflicted the complexity theoretical view of PRAMs

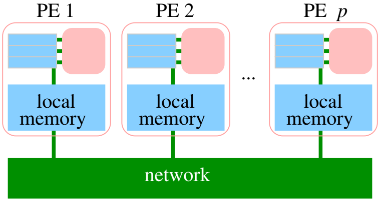
MapReduce – MRC$^+$ Model

Connecting MapReduce to Realistic Machine Models [San20]

internal work

$$\Theta\left(\frac{w}{p} + \hat{w} + \log p\right)$$



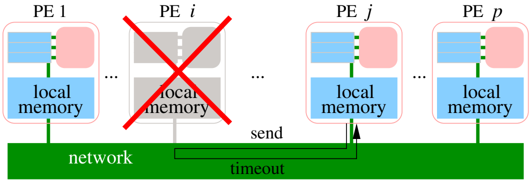


$$\Theta\left(\frac{m}{p} + \hat{m} + \log p\right)$$

bottleneck communication volume

Open Problems

- Apply MRC$^+$ Model to algorithms/problems previously studied for MRC. Are these still looking good? Do they yield new PRAM, BSP, P2P algorithms? Other algorithms now look better?
- Develop sth like MRC$^+$ for Big Data Tools with more functionality like Spark [ZCF$^+$10] or Thrill [BAJ$^+$16]
- Use the algorithms from [San20] to obtain more scalable MapReduce implementations. Possibly further developed with equally scalable fault tolerance.

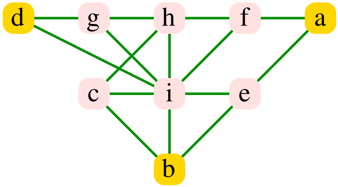


Distributed Graph Algorithms

- "The network is the computer" [Pel00, AW04, Ray13]
- Count rounds of data exchange with all neighbors

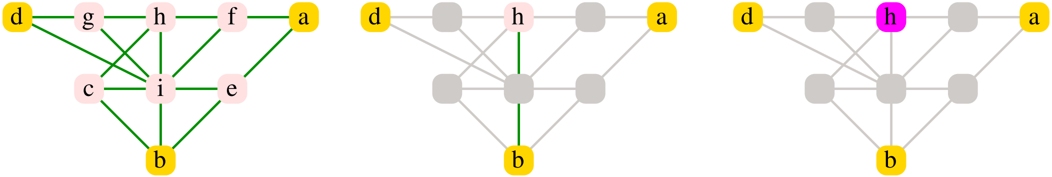
  Local Model: unbounded message lengths

  Congest Model: $\mathrm{O}(\log|V|)$ message lengths
- Quite different from processing graphs $G = (V, E)$ on distributed-memory computers, usually with $p \ll |V|$



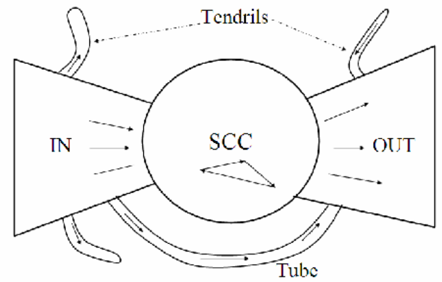
Example:
Luby's Maximal Independent Set Algorithm [Lub86]

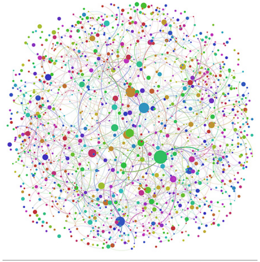
Iteratively select nodes with locally smallest (random) label.
Remove neighbors and incident edges.
whp $\mathrm{O}(\log|V|)$ rounds



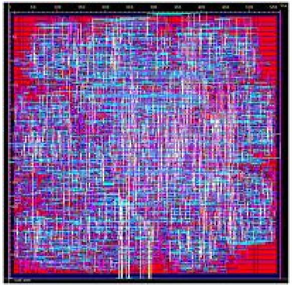
Open Problem

Clarify relation to realistic parallel machine models when processing large graphs, e.g., how to emulate an algorithm in the Congest model on BSP?
How to deal with high-degree nodes?
Which distributed graph algorithms then translate into efficient parallel algorithms?





Data: AER, JPE, Econometrica, RES, QJE (2000-present)
By Cloudly From: www.cloudlychen.net



Overview

From von Neumann to modern machines

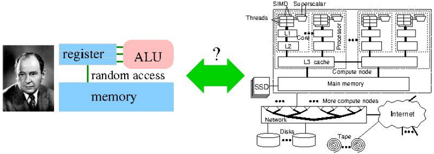
- RAM
- PRAM
- Memory hierarchies
- Distributed memory
- Relations between models

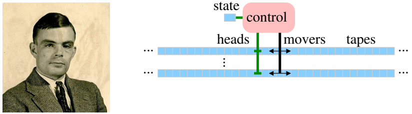
More abstract models

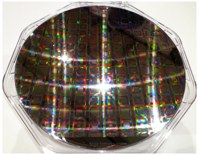
- MapReduce
- Distributed graph algorithms

Wrap Up

- GPU, Quantum, and more
- Open problems
- Future models







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GPU

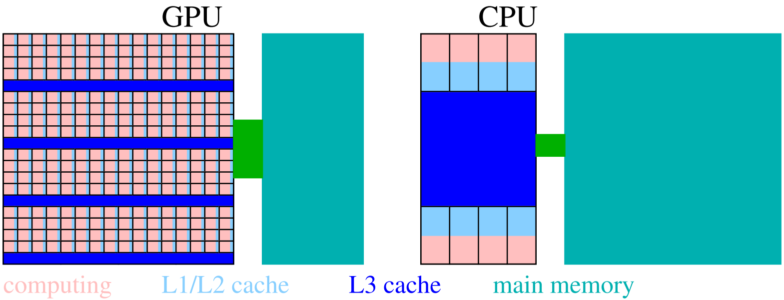
- Hierarchy of thread groups with increasingly closer cooperation
- Collective memory access patterns

Do we need a model for it?

Open problem (?)

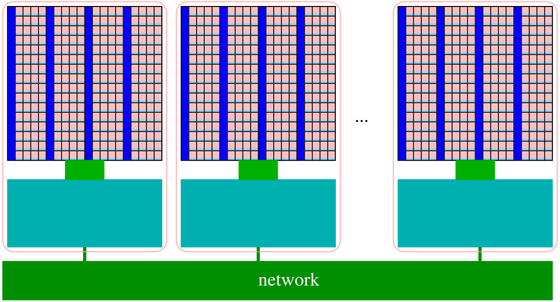
Or not?

- Differences to shared-memory CPUs is more quantitative than qualitative – more threads, smaller caches
- Not that different from a many-core CPU with powerful SIMD-units?
- CUDA is more a programming model than a machine model (and proprietary)
- Ideosyncrasies of warps not fitting to an asymptotic model
- Moving target (and converging to CPU models?)



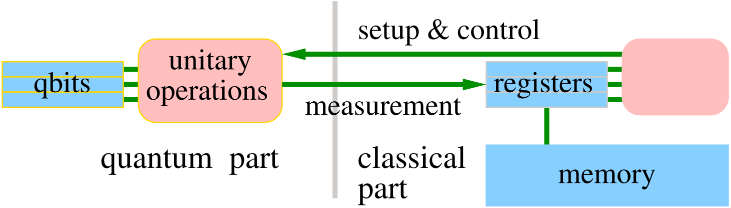
Model LEGO for GPU?

- distributed-memory models for compute nodes
- aCRQW PRAM on each GPU
- broad-word/SIMD parallelism, constant factor things on warp level



Quantum Computing

[Gru99, NC10, Kni96]

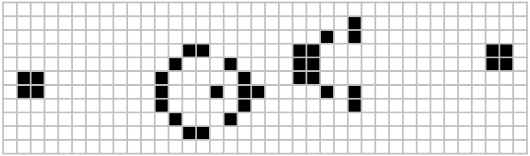


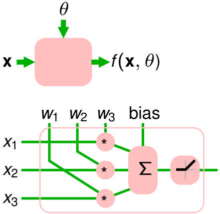
Have size of quantum registers as a parameter?

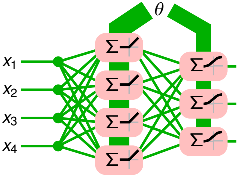
Very different: Quantum annealing – Assume a solver for an NP-hard problem like quadratic unconstrained binary optimization (QUBO)

More from the Zoo

- Reversible computing
- Private computations
- Cellular automata [B+66]
- Molecular computing
- Neural processing
- Peer-to-Peer networks and fault tolerance

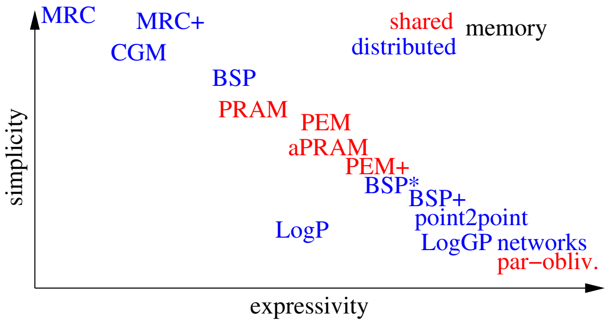






Conclusions

- The zoo is big
- Many models have their point
- But often specifics do not matter
- Tradeoff expressivity versus simplicity



Big Open Problems

Karlsruhe Institute of Technology

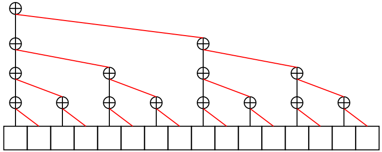
- Classical complexity theory leads to rather coarse grained results.
  Do we need fine-grained complexity of parallel algorithms?
  For example, what about efficient algorithms with span $\mathrm{O}\left(\sqrt{n}\right)$?
- Asymptotics meets hardware design. The quantitative approach [HP17] was highly successful but is hard to extrapolate.
- The asymptotics of physical constraints
  (energy consumption, cooling, wire delays, fault tolerance,...) There was a lot of work on VLSI in the 1980s [Ull84] but that only scratched the surface.
- GPU, quantum, neural
- Would superhuman AIs care about our abstractions?

Exercise: Reduction on aCRQW

Karlsruhe Institute of Technology

Implement $\mathrm{O}(\log p)$ reduction using for the aCRQW model. Perhaps using CAS operations or fetch-and-add.

PE index $i \in \{0, \ldots, n-1\}$
active := 1
for $0 \leq k < \lceil \log n \rceil$ **do**
    (* avoid global barrier here ***)**
    if active **then**
        if bit k of i **then**
            active := 0
        else if $i + 2^k < n$ **then**
            (* ensure that $a[i + 2^k]$ contains the right subtree sum ***)**
            $a[i] := a[i] + a[i + 2^k]$



Exercise: MRC $\rightarrow$ MRC$^+$

Analyze your favorite MRC algorithm using MRC$^+$.
(simple examples: word-count, page-rank).

Sum over all MapReduce steps:

w Total work for μ, ρ

$\hat{w}$ Maximal work for μ, ρ

m Total data volume for $A \cup B \cup C \cup D$

$\hat{m}$ Maximal object size in $A \cup B \cup C \cup D$,

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